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FOR

# METHOD FOR RECONSTRUCTING DATA CLOCKED AT A SYMBOL RATE FROM A DISTORTED ANALOG SIGNAL


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# METHOD FOR RECONSTRUCTING DATA CLOCKED AT A SYMBOL RATE FROM A DISTORTED ANALOG SIGNAL

## Cross Reference to Related Application

This application is a continuation of copending International Application No. PCT/EP02/05106 filed May 8, 2002, and claiming a priority date of May 17, 2001, which designates the United States.

## Technical Field of the Invention

The invention relates to a method and to a device for reconstructing data clocked at a symbol rate, particularly to the purely stochastic data, from an analog signal which has been distorted and attenuated by the transmission of a transmission link.

In digital transmission systems, digital data in the form of rectangular or trapezoidal pulses are fed into a transmission cable, usually a metallic or optical cable and received with a receiver at the other end of the cable. Due to the transmission, the data signal is attenuated with respect to its amplitude and distorted with respect to its phase angle and group delay and, in addition, low- and high-frequency interference can be superimposed. The resultant distorted signal must be amplified and equalized by means of a receiver and the data information must be recovered. For this purpose, known receivers essentially comprise four components, namely an amplifier, an equalizer, a clock recovery circuit and a data recovery circuit.

Figure 2 shows a known receiver for reconstructing data, which is predominantly constructed in analog circuit technology. The receiver path comprises a variable-gain amplifier (VGA) 32 with receiver inputs 30, 31, which amplifies the signal supplied at the input, a noise and crosstalk filter (frequently higher- order low-pass filters) which is constructed as a Bessel filter in this case, and a cable approximation filter 34 implemented as a SC biquad or GmC filter.

Following the cable approximation filter 34, an analog low-pass filter 35 is connected which cuts off higher frequencies, originating from noise and jitter, above the transmission frequency, i.e. the symbol rate and thus suppresses white or colored noise above the data rate.

The optimum case, the overall transfer function of the receiver path up to where the signal is diskretized by a comparator 36 forms the inverse transfer function of the cable of a frequency in amount and phase. As a result, the signal present at input 31, 32 is essentially completely equalized and can be supplied to a data recovery circuit.

To adjust the signal amplitude, the signal is weighted according to the amplitude with the aid of a peak detector or amplitude detector 38 and level detector 39 following the equalizing filter 35, the gain of the amplifier 32 is adjusted in accordance with the amount of the amplitude. Depending on the gain set, the cable approximation filter 34 is matched to the cable transfer function in discrete steps. For this purpose, an equalizer control unit 37 which is connected to the amplifier 32, the cable approximation filter 34, the comparator 36 and the level detector 38 determines the coefficients of the cable approximation in order to duplicate the inverse of the cable transfer function as accurately as possible.

A disadvantage of this analog implementation is, in particular, that the set pole and null positions of the noise and crosstalk filter 2 used and of the cable approximation filter 3 are influenced by parasitic pole and null positions as a result of which the ideal adaptation function of the receiver is correspondingly corrupted.

Furthermore, an analog implementation for equalizing and recovering data is susceptible to production tolerances and applicative variances of the transmission channel. In addition, temperature gradients and mechanical gradients can additionally restrict the operational quality of the sensitive circuits in the receiver and thus impair any error-free recovery of the attenuated and distorted signals.

Furthermore, the number of sets of coefficients for the cable approximation is restricted in analog implementations as a result of which the quality of the cable approximation is also limited. This is because the coefficients of the approximation filter which are determined from a system simulation are only ideal for a particular cable type in a given application condition. Variances in the application conditions such as, e.g. different cable lengths, different temperatures etc often lead to erroneous data detection and thus to higher bit error rates, i.e. to poor data recovery.

Furthermore, it must be noted that, in particular, in the case of great cable lengths or generally in the case of a high cable attenuation, the distance from one interpolation point or set of coefficients to the next interpolation point or set of coefficients is decisive for the error rate due to the $\sqrt{f}$ characteristic, i.e. the dependence of the cable attenuation on frequency and cable length. If the distance between two interpolation points is too great when the cable attenuation is high, the bit error rate rises more than proportionally for intermediate values to the two adjacent interpolation points. To prevent this effect, the distance between interpolation points and thus the sets of coefficients must be reduced, and thus the number of interpolation points must be increased, toward high cable attenuation.

This can be achieved only inadequately due to parasitic influences and properties of analog approaches to equalization.

## Summary of the Invention

It is, therefore, the object of the present invention to improve the quality of equalization and data recovery and to reduce the bit error rate significantly.

An essential concept of the invention consists in implementing most of the elements of the receiver according to the invention in digital circuit technology since the coefficients or parameters for digital elements such as e.g. digital filters can also be changed easily during operation. Incidentally, the compatibility of the receiver

in analog/digital implementation with respect to input jitter is considerably improved by an analog/digital implementation.

The invention provides further advantages by means of the possibility of a simpler implementation of an anti-aliasing filter by means of the oversampling of an analog/digital converter and the possibility of subsequent matching of the circuit to all the characteristics of the transmission channel.

The method according to the invention for reconstructing data from a signal which has been distorted and attenuated by transmission of a transmission link essentially comprises the following steps:

a) amplifying the signal amplitude for compensating for the cable attenuation;
b) filtering of high-frequency interference frequencies above the symbol rate and filtering of low-frequency interference below the lowest spectral component of the useful signal;
c) discretizing the analog signal by means of an oversampled analog/digital converter;
d) forming a cable approximation with the aid of a digitally implemented cable approximation filter in order to obtain an equalized signal; and
e) recovering the data from the equalized signal, the recovered data stream being output, in particular, synchronously with the recovered clock.

According to a preferred embodiment of the invention, an analog/digital converter is used which oversamples the signal n-times and during this process preferably transforms low-frequency noise into higher-frequency spectral noise components above the data rate. Preferably, an SD-ADC (sigma delta analog/digital converter) is used, the specific noise shaping characteristic of which is used by the over-sampling.

This is a further essential aspect of the invention. The oversampling of the signal by an SD-ADC is optimally performed at a minimum sampling rate of $n \geq 8$. The high rate of the sampling rate reduces the requirements for the series-connected anti-aliasing filter with respect to the pole or cut-off frequency and also the stability of the pole frequency. The choice of sampling rate is dependent on the desired noise shaping characteristic of the SD-ADC, the ordinal number to be implemented and the filter type of the anti-aliasing filter and to the subsequent low-pass filtering for delimiting the bandwidth of the signal.

All units following the analog/digital converter up to the data output of the receiver are preferably implemented in digital circuit technology.

The signal output by the analog/digital converter is preferably filtered again by means of a filter (higher-order digital low-pass filter) where, in particular, external (channel) noise, quantization noise and the noise transformed by noise shaping is suppressed above the symbol rate (transmission frequency) and thus the useful signal is band-limited above the symbol rate. In this arrangement, the digital filter preferably has a cut-off frequency which is very narrowly, in particular only 10-20% above or almost at the symbol rate.

According to a preferred embodiment of the invention, the data rate of the signal bandlimited in this manner is produced, by means of a decimator, to a lower clock rate for further processing. In particular, this significantly reduces the circuit complexity (and the power consumption) for a subsequent filter stage.

The subsequent filter stage preferably comprises a digital high-pass filter for suppressing offset and DC components below a predetermined lower cut-off frequency, particularly below the lowest spectral component of the data stream.

According to a preferred embodiment of the invention, a digital cable approximation filter, particularly a FIR (finite impulse response) filter is used for

compensating for the channel distortion. Due to the fact that the data rate has been decimated before the cable approximation filter, the circuit complexity and particularly the area and the current consumption is considerably reduced for this filter.

The transfer characteristic of the cable approximation filter is similar to a high-pass filter due to the duplication of an inverse cable attenuation. This leads to noise caused by a finite word length (quantization noise) and/or finite word width of the coefficients within the useful signal spectrum to be adapted being amplified. This characteristic is generally called noise enhancement. Attention must be paid to the fact that the word width is sufficiently long since the filter implementation is based on computing operations.

The gain of the amplifier stage at the receiver input and the characteristic of the digital cable approximation filter can be adjusted and adapted to altered application conditions even in operation.

According to a preferred embodiment of the invention, the amplifier stage and the digital cable approximation filter are controlled by an equalizer control unit which selects and sets the optimum set of filter coefficients for the digital cable approximation filter in dependence on the signal amplitude.

The data for the digital cable approximation filter are preferably stored in a RAM or ROM memory but can also be loaded from an external source via a digital interface.

According to a preferred embodiment, the data rate of the equalized signal is increased after the cable approximation filter in order to improve the subsequent clock and data recovery. For this purpose, an interpolation and filter unit is preferably provided which has a further digital low-pass filter for suppressing

frequency components above the symbol rate which have been produced mainly by the interpolation.

The interpolation and filter unit is preferably located outside the control loop of a subsequent digital phase-locked loop for data recovery.

Phase-locked loops or PLL circuits are circuits for synchronizing the frequency and phase of two signal oscillations, particularly of clock signals. The output clock signal output at the output of the phase-locked loop is synchronous to the input clock signal present at the input in normal operation.

The control loop of the phase-locked loop preferably comprises a decimator, a phase detector and a device for setting the clock and phase control characteristic, particularly a timing loop filter. According to a preferred embodiment of the invention, the amplitude threshold value used in the phase detector is controlled by a peak detector (amplitude detector).

Furthermore, the digital phase-locked loop preferably comprises a unit for synchronizing the output data and a digitally controlled oscillator for generating the regenerated clock, the unit for synchronizing the output data supplying a data stream output synchronously with the clock of the oscillator.

An essential aspect of the PLL circuit according to the invention is a decimator arranged at the input of the phase-locked loop. The phase-locked loop requires that, depending on the phase angle with respect to the clock synchronization, a sample with the correct phase angle is selected from the data stream. This function is combined with a decimator for reducing the clock rate. The low-pass characteristic of the decimator is used for the additional suppression of noise components. Furthermore, the advantage lies in the reduction of the clock rate and of the required area and power consumption of the subsequent circuits.

The device according to the invention for reconstructing data from a signal which has been distorted by transmission over a transmission link comprises the following:

a) a programmable amplifier for compensating for the cable attenuation;
b) a low-pass filter for suppressing high-frequency interferers above the symbol rate, which is constructed as an analog anti-aliasing and crosstalk filter;
c) an oversampled analog/digital converter with noise-shaping characteristic for discretizing the analog signal;
d) a digitally implemented cable approximation filter for obtaining an equalized signal; and
e) a preferably digital phase-locked loop for recovering the data and the clock from the equalized signal.

The device according to the invention preferably also comprises

f) a low-pass filter for suppressing high-frequency interference frequencies above the symbol rate, which is preferably constructed as a digital noise and cross talk filter.
g) a high-pass filter for suppressing low-frequency interferers below the lowest spectral components of the useful signal;
h) a decimator for reducing the clock rate; and
i) an interpolator followed by a low-pass filter for increasing the clock rate and as a shaping filter.

Brief Description of the Drawings

In the text which follows, the invention will be explained in greater detail by way of example by means of the attached figures, in which:

**Fig. 1** shows a predominantly digitally implemented receiver according to an exemplary embodiment of the invention;

**Fig. 2** shows a known receiver predominantly constructed by means of analog circuit technology.

Detailed Description of the Preferred Embodiments

The receiver path of the equalizer 10 of Fig. 1 comprises (from the left to the right) an amplifier which is constructed as VGA Stage 1 and an analog low-pass filter 2 which forms an anti-aliasing and crosstalk filter for a subsequent oversampled analog/digital converter 3.

A low-pass filter 4, connected to the analog/digital converter 3, is used for suppressing noise components above the symbol rate and for limiting the signal bandwidth above this fundamental frequency, as a result of which external noise, quantization noise and the noise transformed by noise shaping is suppressed.

The analog/digital converter is constructed as SD-ADC (sigma-delta ADC) which oversamples the supplied signal n-times. Due to the oversampling, the noise-shaping characteristic of the converter is utilized.

To reduce the data rate by factor m, where, preferably, m = 5-10, a digital decimator 5 is provided which is arranged between the digital low-pass filter 4 and a digital cable approximation filter 7.

A digital high-pass filter connected to the decimator 5 is used for filtering low-frequency noise and for offset and DC component suppression below the lowest spectral component of the data stream.

The output of the equalizer 10 forms a digital FIR filter 7 as a cable approximation filter for compensating for the cable distortion.

Furthermore, a digital equalizer control unit 8 is provided which controls the amplifier 1 and the FIR filter in dependence on the signal amplitude.

The equalized signal output at the output of the equalizer 10 is, in particular, linearly interpolated and limited in its bandwidth by means of an interpolation and filter unit 19 comprising an interpolation unit 11 and a low-pass filter 12. In this arrangement, the low-pass filter 12 is used for suppressing frequency components above the symbol rate which, in particular, have been produced by the interpolation.

The receiver also comprises a digital phase-locked loop comprising a decimator 13 which forms a part of the phase-locked loop. The control loop also comprises a phase detector 15 for determining the phase error of the detected data with reference to the recovered clock and a timing loop filter for adjusting the clock control characteristic.

The timing loop filter 17 is connected to the phase detector 15, the decimator 13 and a controlled oscillator 18 for generating the regenerated clock. The phase detector 15 is connected to the decimator 13, the timing loop filter 17, a peak detector 14 for readjusting the threshold value used in the phase detector 15, and a synchronization device 16 which supplies at the data output (data) a data stream which is synchronous with the clock of the oscillator 18. The clock is output at the clock output (clock).

With respect to the known receiver shown in Figure 2, reference is made to the introduction to the description.